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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/593,912	06/14/2000	Yatin R. Acharya	E0897	8324

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EXAMINER	
YAO, KWANG BIN	

ART UNIT	PAPER NUMBER
2667	5

DATE MAILED: 02/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/593,912	ACHARYA, YATIN R.	
	Examiner	Art Unit	
	Kwang B. Yao	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *19-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Engdahl et al. (US 5,493,571).

Engdahl et al. discloses an apparatus for digital communication comprising the following features: regarding claim 1, a system in a media access controller (Figs. 5A and 5B, REF 100) for communicating to a number of physical layer devices (I/O device), comprising: a common bus port for electrical coupling to a common bus (101) that is electrically coupled to the physical layer devices (I/O device), the common bus serving as a direct interface between the data link layer and physical layer; logical circuitry to transmit a training sequence from the common bus port (Fig. 5A REF 103) to the physical layer devices (I/O device); and logical circuitry (Fig. 5B, REF 141) to transmit a data block from the common bus port to a respective one of the physical layer devices by way of the common bus (101), the data block being transmitted in one of a number of time slots of a time division multiplexed transmission; regarding claim 2, wherein the logical circuitry (Fig. 5B, REF 141) to transmit a training sequence from the common bus port further comprises logical circuitry to transmit a transmit enable signal (Fig. 7, TX ENABLE) from the common bus port simultaneously with the data block (Fig. 7, TX PHY SYMBOLS) ,

thereby indicating a transmission of the data block to the physical layer devices (I/O device); regarding claim 3, wherein the logical circuitry (Fig. 5B, REF 141) to transmit a training sequence from the common bus port to the physical layer devices(Fig. 1, REF 12-16) further comprises logical circuitry (Fig. 5B, REF 141) to transmit an address designation (Fig. 2A, REF 24) in each of the time slots (Fig. 3); regarding claim 4, wherein the logical circuitry to transmit a training sequence from the common bus port to the physical layer devices further comprises logical circuitry to transmit a predefined training sequence (Fig. 2A) that provides a reference for the time slots (Fig. 3); regarding claim 5, wherein each of the address designations (Fig. 2A, REF 24) is transmitted in a first portion of the corresponding time slot; regarding claim 6, wherein a predetermined sequence (Fig. 2A, REF 25) is transmitted in a second portion of the corresponding time slot; regarding claim 7, (as described on column 26-30), a system in a media access controller (Figs. 5A and 5B, REF 100) for communicating to a number of physical layer devices (I/O device), comprising: a processor (Fig. 10, REF 400) coupled to a local interface (Fig. 5B, REF 143); a memory (Fig. 10, REF 411) coupled to the local interface (Fig. 5B, REF 143); a common bus port coupled to the local interface, the common bus port being adapted for electrical coupling to a common bus (101) that is electrically coupled to the number of physical layer devices (I/O device), the common bus serving as a direct interface between the data link layer and physical layer; and operating logic stored on the memory (Fig. 10, REF 411) and executable by the processor (Fig. 10, REF 400), the operating logic further comprising: logic (Fig. 10, REF 401) to transmit a training sequence from the common bus port to the physical layer devices; and logic (Fig. 10, REF 401) to transmit a data block from the common bus port to a respective one of the physical layer devices by way of the common bus, the data block being

transmitted in one of a number of time slots of a time division multiplexed transmission; regarding claim 8, wherein the logic (Fig. 10, REF 401) to transmit a training sequence from the common bus port to the physical layer devices further comprises logic to transmit a transmit enable signal from the common bus port simultaneously with the data block, thereby indicating a transmission of the data block to the physical layer devices; regarding claim 9, wherein the logic (Fig. 10, REF 401) to transmit a training sequence from the common bus port to the physical layer devices (I/O device) further comprises logic to transmit an address designation (Fig. 2A, REF 24) in each of the time slots; regarding claim 10, wherein the logic (Fig. 10, REF 401) to transmit a training sequence from the common bus port to the physical layer devices (I/O device) further comprises logic to transmit a predefined training sequence (Fig. 2A) that provides a reference for the time slots (Fig. 3); regarding claim 11, wherein each of the address designations (Fig. 2A, REF 24) is transmitted in a first portion of the corresponding time slot; regarding claim 12, wherein a predetermined sequence (Fig. 2A, REF 25) is transmitted in a second portion of the corresponding time slot; regarding claim 13, a system in a media access controller (Figs. 5A and 5B, REF 100) for communicating to a number of physical layer devices (I/O device), comprising: a common bus port coupled to the local interface (Fig. 3, REF 143), the common bus port being adapted for electrical coupling to a common bus (101) that is electrically coupled to the number of physical layer devices (I/O device), the common bus serving as a direct interface between the data link layer and physical layer; means for transmitting (Fig. 5A, REF 141) a training sequence from the common bus port to the physical layer devices (I/O device); and means for transmitting (Fig. 5B, REF 141) a data block from the common bus port to a respective one of the physical layer devices (I/O device) by way of the common bus (101), the

data block being transmitted in one of a number of time slots of a time division multiplexed transmission; regarding claim 14, wherein the means for transmitting (Fig. 5B, REF 141) a training sequence from the common bus port to the physical layer devices (I/O device) further comprises means for transmitting a transmit enable signal (Fig, 7, TX ENABLE) from the common bus port simultaneously with the data block (FIG. 7, TX PHY SYMBOLS), thereby indicating a transmission of the data block to the physical layer devices (I/O device); regarding claim 15, wherein the means for transmitting a training sequence from the common bus port to the physical layer devices further comprises means for transmitting an address designation (Fig. 2A, REF 24) in each of the time slots (Fig. 3); regarding claim 16, a method in a media access controller (Figs. 5A and 5B, REF 100) for communicating to a number of physical layer devices (I/O device), comprising the steps of: transmitting a training sequence to the physical layer devices by way of a common bus (101), the common bus serving as a direct interface between the data link layer and physical layer; and transmitting a data block to a respective one of the physical layer devices (I/O device) by way of the common bus, the data block being transmitted in one of a number of time slots of a time division multiplexed transmission; regarding claim 17, wherein the step of transmitting a training sequence to the physical layer devices (I/O device) by way of a common bus (101) further comprises the step of transmitting a transmit enable signal (Fig, 7, TX ENABLE) to the physical layer devices (I/O device) by way of the common bus (101) simultaneously with the transmission of the data block, thereby indicating a transmission of the data block to the physical layer devices (I/O device); regarding claim 18, wherein the step of transmitting a training sequence to the physical layer devices (I/O device) by way of a common bus (101) further comprises the step of transmitting an address designation (Fig. 2A,

REF 24) in each of the time slots (Fig. 3). See column 1, lines 18-29; column 5-34; column 35, lines 23-40.

Response to Arguments

3. Applicant's arguments filed 11/26/03 have been fully considered but they are not persuasive.

On page 10, fifth paragraph, Applicant argues that the present invention is significantly different from that which is taught in Engdahl et al.; that is because Engdahl et al. is concerned with TDM on a completely different level, i.e., the network level, rather than the interface between the data link layer and the physical layer as in the presently claimed invention. Examiner respectfully disagrees with these arguments. The I/O devices (claimed physical layer devices) connected to the I/O node 16 in Fig. 1 are physical layer devices. The host bus 101 in Figs. 5A and 5B is the common bus serving as a direct interface between the SMAC 100 and I/O devices. See column 1, lines 18-29; column 35, lines 23-40. Therefore, it is respectfully submitted that the reference of Engdahl et al. does anticipate the claimed invention.

On page 11, first paragraph, Applicant argues that Engdahl et al. does not teach or suggest time division multiplexed communication between a MAC and a number of physical layer devices along a common bus servicing as a direct interface between the data link layer and the physical layer. Examiner respectfully disagrees with these arguments. The I/O devices (claimed physical layer devices) connected to the I/O node 16 in Fig. 1 are physical layer devices. The host bus 101 in Figs. 5A and 5B is the common bus serving as a direct interface between the SMAC 100 and I/O devices. See column 1, lines 18-29; column 35, lines 23-40.

Therefore, it is respectfully submitted that the reference of Engdahl et al. does anticipate the claimed invention.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kwang B. Yao whose telephone number is 703-308-7583. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H Pham can be reached on 703-305-4378. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KWANG BIN YAO
PRIMARY EXAMINER

Kwang B. Yao
Feb. 4, 2004